Reviewed by: Andrew Newman

Module Name:Tx/Rx FIFO

Jira Ticket:[CAN2-18]

**CAN Controller Requirements Checklist Rev.1**

1. Is requirements document written clearly and grammatically correct?

Yes [ ] No [x]

Comments: FIFO\_W\_01 change w\_en to i\_w\_en.

FIFO\_W\_03 and FIFO\_R\_03 change “equal to 1 less than the buffer length” to “equal to FIFO\_DEPTH-1”.

1. Does requirements document define all functions to be performed by the module?

Yes [ ] No [x]

Comments: Initialization is missing reqs for all of the outputs of the module.

1. Does requirements document include all inputs and outputs to the module along with their corresponding accuracy, range of values, frequency and format?

Yes [ ] No [x]

Comments:Missing definitions for o\_overflow, o\_underflow.   
In FIFO\_W\_03, r\_ptr would not always reside at 0. Consider case where there are concurrent reads and writes, with writes occurring more often. Flag would not be set most of the time. Same goes for FIFO\_R\_03. Look at the example implementation with differential pointer for inspiration on how to describe this better.

1. Is each requirement unique?

Yes [x] No [ ]

Comments:

1. Does requirements document comply with system requirements and traceability?

Yes [ ] No [x]

Comments: See 3.

1. Is terminology consistent with Requirements Standards?

Yes [x] No [ ]

Comments:

1. Is it possible to implement all requirements?

Yes [x] No [ ]

Comments:

1. Is each requirement testable or verifiable?

Yes [x] No [ ]

Comments: